Structurally Programmable Channel Decoder for Digital Broadcast Reception

ABSTRACT OF THE DISCLOSURE

An architecture is provided that includes a reconfigurable bridge for routing data among functional units. Register transfer units effect the routing of data among registers that are associated with each functional unit. Synchronous and asynchronous register transfers are supported, including interrupt signal generation for efficient digital signal processor support. A preferred embodiment of the reconfigurable bridge includes a plurality of reconfigurable datapath units that provide ancillary functions to facilitate the processing and pre-processing of data items as they are transferred among registers. A preferred embodiment of the invention also includes an instruction memory that contains instructions to effect the desired register transfers and ancillary operations.